NASA's 3D Flight Computer for Space Applications

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Abstract

The New Millennium Program (NMP) Integrated Product Development Team (IPDT) for Microelectronics Systems was planning to validate a newly developed *3D Flight Computer* system on its first deep-space flight, DS1, launched in October 1998. This computer, developed in the 1995-97 time frame, contains many new computer technologies previously never used in deep-space systems. They include: advanced 3D packaging architecture for future low-mass and low-volume avionics systems; high-density 3D packaged chip-stacks for both volatile and non-volatile mass memory: 400 Mbytes of local DRAM memory, and 128 Mbytes of Flash memory; high-bandwidth Peripheral Component Interface (PCI) local-bus with a bridge to VME; high-bandwidth (20 Mbps) fiber-optic serial bus; and other attributes, such as standard support for Design for Testability (DFT). Even though this computer system did not complete on time for delivery to the DS1 project, it was an important development along a technology roadmap towards highly integrated and highly miniaturized avionics systems for deep-space applications. This continued technology development is now being performed by NASA's **Deep Space System Development Program** (also known as **X2000**) and within JPL's Center for Integrated Space Microsystems (CISM).

Keywords:
New Millenium Program, Flight Computer, Avionics.

Introduction

As part of NASA's New Millennium Program (NMP) to validate technologies for space flight missions in the new millennium, the Integrated Product Development Team (IPDT) for Microelectronics Systems developed the *3D Flight Computer*, as a general-purpose space computer [1], [2]. In 1995, this computer system was selected for validation on the first deep-space mission, DS1, which launched in October 1998. However, due to delays in the delivery of the technology to the project, in March of 1997, the 3D Flight Computer was 'de-manifested', and replaced with off-the-shelf technology.

Other technologies from the Microelectronics Systems IPDT such as the Ultra Low-Power Experiment (ULPExp) which evaluates 0.25u Silicon on Insulator (SOI) technology from MIT/LL, and the Power Activation and Switching Module (PASM) from Lockheed Martin and Boeing, were delivered on time for integration on the spacecraft, and are currently being validated as part of the DS1 mission.

The 3D Flight Computer was developed in partnership with industry and academia in the 1995-1997 time frame. The partners included: Lockheed Martin Federal Systems for the CPU and local memory; TRW for the non-volatile memory module; Boeing for the I/O module, including the high-bandwidth fiber-optic interface; Space Computer Corporation (SCC) for the 3D packaging technology; and Georgia Institute of Technology for the Design for Testability technology.

Even though the 3D Flight Computer was not delivered on time for integration on the DS1 spacecraft, this development represents a significant technology milestone. Moreover, the technology vision and roadmap developed by the

Microelectronics Systems IPDT is further being developed by the newly formed NASA Deep Space Systems Program (also known as X2000), at the Center for Integrated Space Microsystems (CISM) at the Jet Propulsion Laboratory [4].

In the remainder of this paper, we first describe the 'technology push' that the 3D Flight Computer represents, for the 95-97 time frame. Following this, in Section 3, we describe the computer system architecture, which is based on Commercial Off The Shelf (COTS) interfaces. In Section 4, we describe the 3D Flight Computer packaging architecture, followed by a status of the qualification tests performed. Finally, we provide our concluding observations, leading into the newly formed Deep Space Systems Development Program (X2000), and the Center for Integrated Space Microsystems. This is a new center for the technology development of advanced micro-avionics systems. Much of the work being performed by X2000 at CISM has directly benefited from prior investments by the NMP in the area of advanced computer systems.

2. *3D Flight Computer* Technologies

The Microelectronics Systems roadmap developed by the IPDT addressed a number of different technology areas [3], including:

- deep sub-micron radiation tolerant semiconductor foundries;
- processor technologies and ISAs;
- memory technologies, including both volatile and non-volatile memory;
- I/O technologies including low-bandwidth engineering requirements, and high-bandwidth instrument requirements and local device requirements;
- advanced packaging technologies for chip-scale packaging and 3D packaging at the die level, multi-chip module level, and the system level;
- power management and distribution for high levels of integration, high-efficiency, as well as power efficient distribution architectures;
- design capabilities including Design For Testability and design for low-power;
- low-cost design, manufacturing, system integration and test, etc.

The following is a list of new technologies that have been incorporated as part of the 3D Flight Computer:

1. The 0.5-micron bulk-CMOS radiation hard semiconductor foundry at Lockheed Martin Federal Systems in Mannasas, Virginia, was the most advanced foundry for space applications in 1995 available to NASA. In fact, this technology was only one generation behind the most advanced commercial semiconductor technology. Labeled as CMOS-5L, the 0.5 micron CMOS technology was used for the development of the computer Central Processing Unit (CPU).
2. RAD6000-5L is a radiation hard CPU operating at a maximum rate of 50 MHz. A PowerPC (PPC) was also considered, but was not available on time.
3. 400 Mbytes of local memory using five 3D-DRAM stacks. Each DRAM stack consists of 40 usable 16 Mbit die assembled in a single 'sugar-cube' of silicon. Each cube actually stacks 48 die, of which 40 useful ones are selected. Each stack thus provides 80 MB of storage. 80 MB of the total 400 MB is used for EDAC, for a total of 320 MB of effective data storage. The memory cubes were also from LM Federal Systems.
4. 128 Mbytes of non-volatile memory in 4-high stacks of Flash memory from TRW.
5. Peripheral Component Interface (PCI) as the Commercial-Off-The-Shelf (COTS) local bus with a VME bridge.
6. Advanced I/O module that provides both the PCI local bus and the PCI to VME Bridge in a single computer slice. The same slice also provides the 1773 high-bandwidth (20 Mbps) serial fiber optic interface to the rest of the spacecraft.
7. 3D Packaging technology enables the compact size and reduced volume of the complete stand-alone computer system. 3D packaging is used at three levels: die or chip stacking; multi-chip modules; and 3D stacking of computer 'slices' with vertical interconnects between slices.
8. An innovative approach to Design for Testability was also integrated into the design from Georgia Institute of Technology [5].

3. Flight Computer Architecture

In Figure 1, we show the diagram of the 3D Flight Computer architecture. All of the interfaces in this computer are based on commercial-off-the-shelf (COTS) technology, including: the PCI local bus interface, the VME system bus interface, the high-

bandwidth serial fiber-optic interface, and the JTAG test bus interface. Using exclusively commercially defined interfaces was intended to reduce the cost of design, integration and test, support equipment development, as well as manufacturing costs.

As shown, the 3D-flight computer offers both PCI and VME parallel interfaces to local devices or other system modules. The computer can be used as a stand-alone system with only the serial fiber-optic interface leading to remote terminals, or the computer can be mounted onto other standard boards, such as PCI or VME. The addition of the VME Bridge to the computer module was done so that the computer module can integrate into a VME-based system with other existing VME boards. This feature can also be used during integration and test, if existing VME based support equipment is available. The computer runs the VxWorks operating system with support for the C programming language.

As proposed, the 3D Flight Computer was intended to be a single computer node in a distributed fault-tolerant architecture. That is, multiple compute nodes would be connected over the high-bandwidth serial bus to offer distributed fault-tolerant services to the spacecraft. This distributed architecture is currently the baseline for X2000 First Delivery Project under development at JPL for the Outer Planets and Solar Probe programs.

4. Computer Packaging Approach

Since advanced avionics miniaturization was one of the essential components of the Microelectronics Systems IPDT roadmap, a special emphasis was placed on advanced packaging technologies. This included three distinct technology areas:

- 3D packaging for both bare die and packaged die;
- multi-chip modules (MCM);
- 3D packaging of MCMs.

An early graphical depiction of the flight computer packaging approach is shown in Figure 2 below. Shown are four separate computer modules or 'slices', assembled into a 3D configuration proposed by Space Computer Corporation (SCC): the processor slice, local memory slice, non-volatile memory slice, and the I/O slice, are each mounted separately on printed circuit boards, which are then mechanically stacked. The data interconnect between each computer slice is performed using elastomerics and fine-pitch wires. Two kinds of connectors were evaluated: ETI Matrix MOE, and Ampliflex connectors. Figures 3-5 show photos of the actual 3D Flight Computer system during test in the lab.

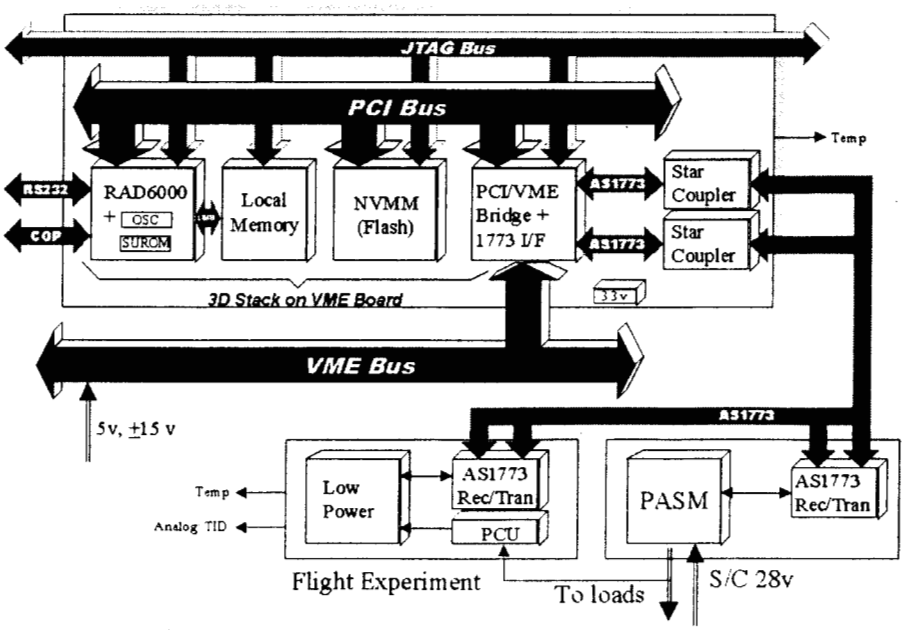

Figure 1:Microelectronics NMP-DS1 Block Diagram

5. Status of Qualification

The qualification tests on the 3D Flight Computer included vibration, thermal vacuum, thermal cycling, and accelerated aging (stress relaxation of elastomeric) at high temperatures [6]. The following is a summary of the qualification test results:

- vibration testing: no electrical or mechanical failures;
- thermal vacuum: slightly better than expected heat transfer from MCMs to VME cold plate;
- thermal cycling: dual-row ETI material displayed open circuits at low temperature (-29 degree C). Single row ETI operational from –55 to 80 degree C. Ampliflex material operational from –50 to 80 degree C.
- Accelerated aging: Ampliflex material displayed no opens after temperature soak at 150 degrees C. Single row ETI material exhibited opens and higher temperature resistance contacts after temperature soak at 125 degrees C.

Therefore, based on the Qual Stack tests, the 3D MCM stack technology has been validated with the Ampliflex elastomeric conncectors.

6. Conclusions

The 3D Flight Computer developed for the NMP DS1 spacecraft contains numerous advanced avionics technologies. Even though the advanced computer system was not delivered on time for integration onto the DS1 spacecraft, this technology development represents a significant technology achievement by the Microelectronics IPDT. Results of this technology development have been integrated into the newly formed Deep Space Systems Program at JPL's Center for Integrated Space Microsystems (CISM).

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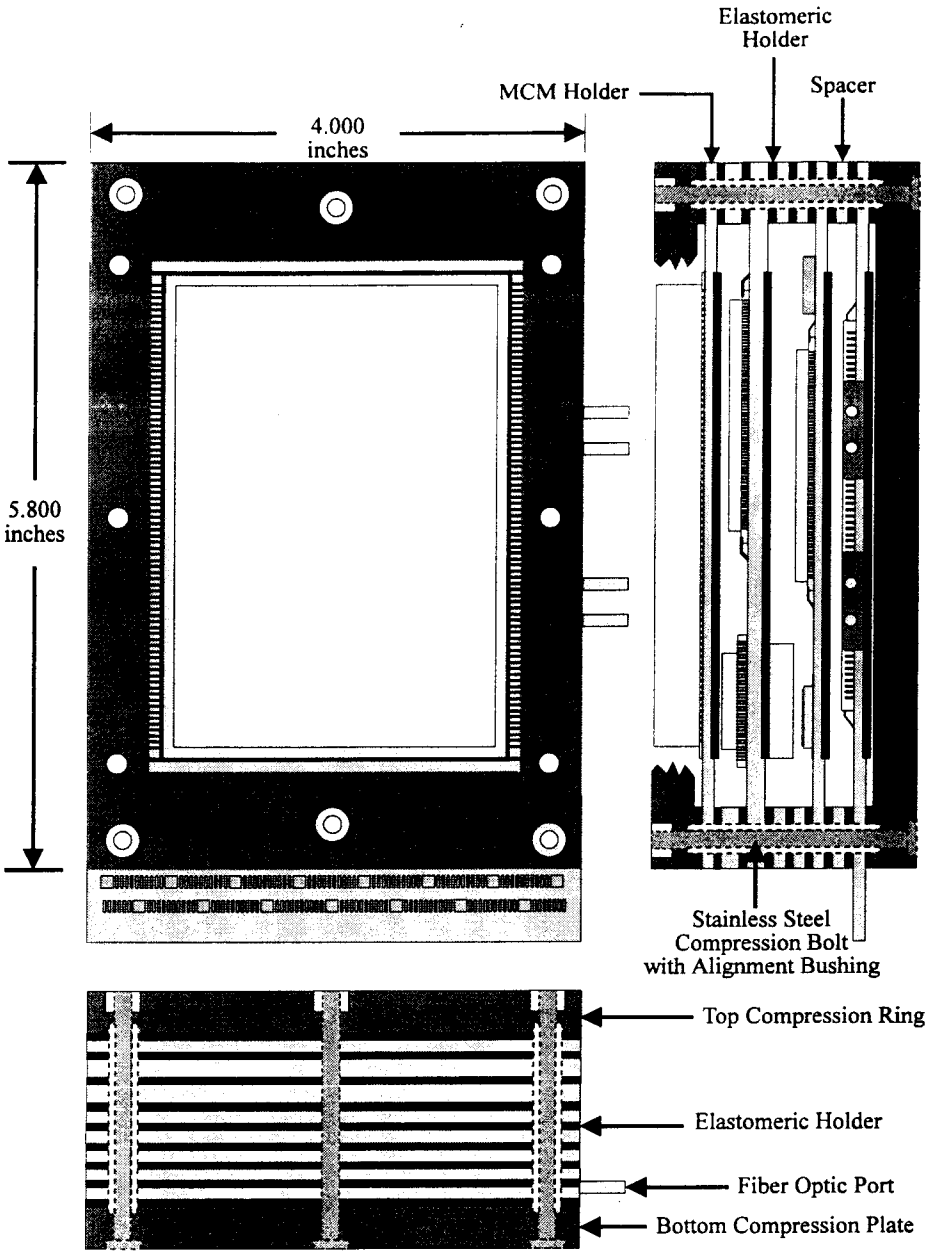

Figure 2 - 3D Stack with Side Plates Removed

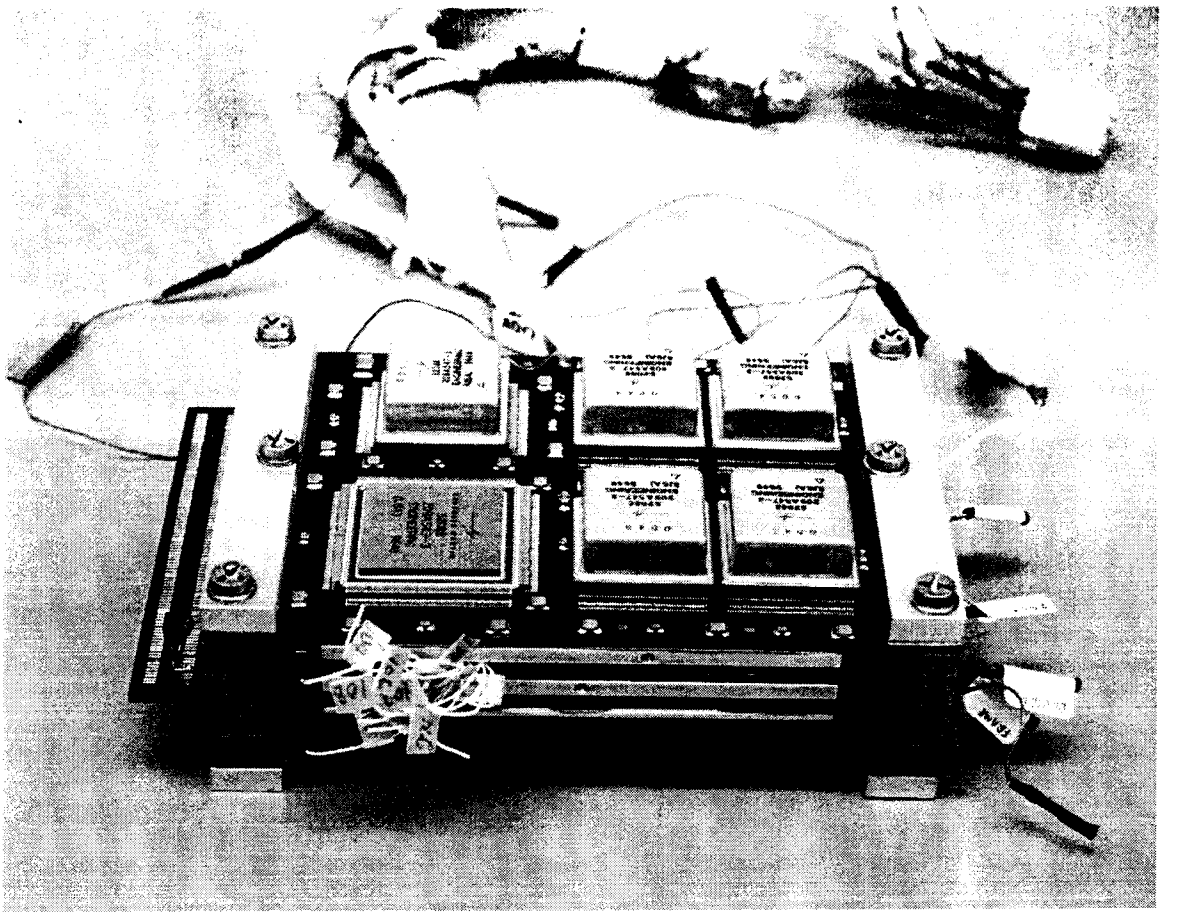

Figure 3 - 3D Flight Computer

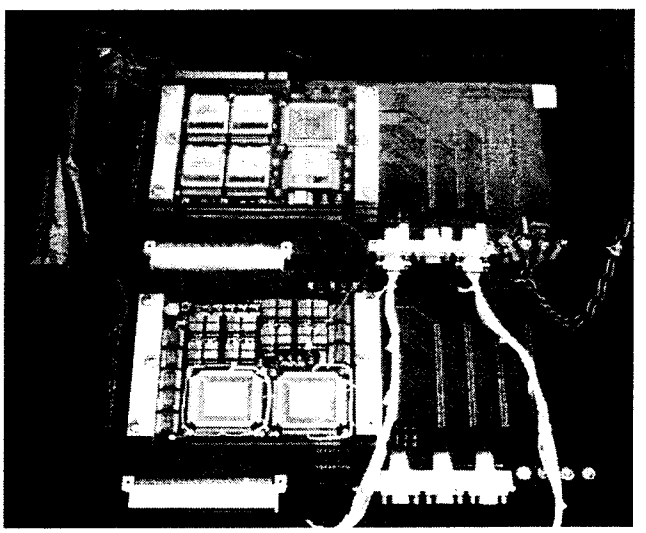

Figure 4 - Slices of 3D Flight Computer

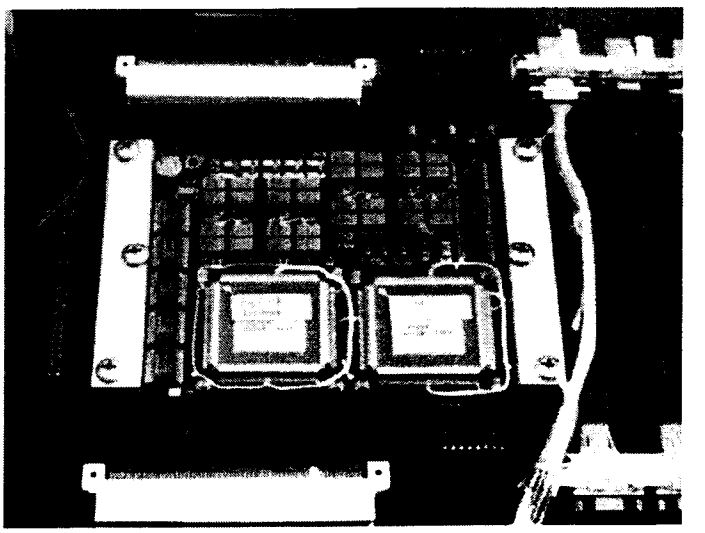

Figure 5 - Slice of 3D Flight Computer